steps wherein photoresist masks PM1, PM6 and PM7 were applied. Applicants are also amending the specification to reflect the new numbering of these drawings.[1] It is believed that no new matter is being added. Applicants respectfully submit that this overcomes the Examiner's objection and request that this objection be withdrawn.

II. Claim Rejections - 35 USC §112

The Examiner rejects Claims 25 and 27 under 35 USC §112, second paragraph, as being indefinite. In particular, the Examiner states:

> "It is not clear how the claimed semiconductor device could be a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disc player, an electronic game machine or a projector. How could this device be a personal computer?" (pages 2-3)

Applicants respectfully submit that the term "semiconductor device" is clearly defined on the first page of the specification. In particular, the specification states:

> "Note that the term "semiconductor device" used herein represents those devices which operate by utilizing semiconductor characteristics, and embraces within its scope the electro-optical devices as well as the electronic appliances incorporating the electro-optical device that are described above. (page 1, lns. 6-13)"

Applicants further define this definition on pages 46-47 of the specification as follows:

> "The active matrix substrate, the liquid crystal display device and the EL display device fabricating in accordance with the present invention can be used for various electro-optical devices. The present invention can be applied to all those electronic appliances that include such an electro-optical device as the display medium. Examples of the electronic appliances include a personal computer, a digital camera, a video camera, a portable information terminal (a

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[1] Unfortunately, the undersigned does not have an electronic copy of the specification to make the corrections therein. Therefore, a marked-up copy is being submitted herewith. As soon as the undersigned receives the electronic copy of the specification, he will submit the corrected paragraphs of the specification.

> mobile computer, a cellular telephone, an electronic book), and a navigation system. Fig. 22A to 22F show examples of these." (page 46, ln. 23 - page 47, ln. 6).

Hence, it is clear from these passages that the use of the term "semiconductor device" in Claims 25 and 27 means a device which either has semiconductor characteristics or incorporates the semiconductor device of the present invention therein.[2] Therefore, this term is not indefinite in these claims.

However, in accordance with the Patent Office's business policy and in order to advance the prosecution of this application, Applicants have amended Claims 25 and 27[3] to state

> "wherein the semiconductor device is <u>in an apparatus</u> selected from a group consisting of a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disc player, an electronic game machine and a projector."

It is respectfully submitted that this rejection has now been overcome and should be withdrawn.

III. <u>Claim Rejections - 35 USC §103</u>

The Examiner has the following rejections under 35 USC §103:

a. Claims 1 and 25 as being unpatentable over Matsumoto in view of Adan et al. and Shimone;

b. Claims 3 and 27 as being unpatentable over Matsumoto in view of Adan et al., Shimone and Karauchi et al.; and

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[2] The Examiner appears to recognize this definition in his §103 rejection of Claim 25 at page 5 wherein he states "[w]ith regard to claim 25, the semiconductor device of Matsumoto, Adan and Shimone could obviously be part of a personal computer." Though, as explained *infra*, Applicants disagree with this rejection.

[3] As this amendment is merely to clarify the language in the claim, Applicants do not believe that the amendment is a Festo-type narrowing amendment.

c. Claims 21 and 23 as being unpatentable over Matsumoto in view of Adan et al., Shimone, and Karauchi et al. and further in view of Hioki.

Each of these rejections is respectfully traversed.

The present invention of independent Claims 1 and 3 (and new independent Claim 53) is directed to a semiconductor device having a pixel TFT and a driver circuit comprising a p-channel TFT and an n-channel TFT, over a substrate. The pixel TFT has a channel forming region and a LDD region. The n-channel TFT of the driver circuit has a LDD region that partly overlaps a gate electrode. The p-channel TFT of the driver circuit has a channel forming region and a p-type impurity region that forms a source region or drain region and is disposed in contact with the channel forming region. The p-channel TFT of the driver circuit does not have a LDD region.

In contrast, Matsumoto discloses a semiconductor structure which is "LDD(Lightly Doped Drain) structured" (Col. 3, lns. 10-11). The structure of Matsumoto has a pixel section having a pixel TFT (21) and a driver circuit comprising a p-channel TFT (23) and an n-channel TFT (22). Each of these TFTs (21-23) has a LDD structure (see col. 3). Further, as the Examiner acknowledges, Matsumoto does not disclose or suggest a n-channel TFT having a LDD region which partly overlaps a gate electrode.

The Examiner then cites Adan and specifically Fig. 29 therein. However, while Fig. 29 discloses a LDD region (71) partly overlapping a gate electrode (66), Applicants believe that there is no indication in Adan as to what TFTs have a LDD region nor is there any suggestion of a TFT without a LDD region.

Hence, even if the two references are combined, which Applicants do not agree is proper, the combination would still fail to disclose or suggest a pixel TFT that is an n-channel TFT and has a LDD region, and a driver circuit with an n-channel TFT having a LDD region which partially

overlaps a gate electrode and a p-channel TFT which does not have a LDD region. The other cited references also do not appear to disclose or suggest this point.

Therefore, it is respectfully submitted that the claims of the present application are not disclosed or suggested by the cited references but are patentable thereover. Accordingly, it is requested that they now be allowed.

Additionally, Claim 53 has been added to claim the features of Fig. 11. Please charge our deposit account 50/1039 for the fee for this claim and any further fee for this amendment.

It is respectfully submitted that the present application is now in a condition for allowance and should be allowed.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

Date: March 11, 2002

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Registration No. 34,225

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Marked-up copy of the claims as amended:

IN THE CLAIMS:

Please amend the claims as follows:

1. (Amended) A semiconductor device comprising:

a pixel TFT disposed in a pixel section; and

a driver circuit comprising a p-channel TFT and an n-channel TFT,

over a substrate,

wherein:

the p-channel TFT of the driver circuit comprises a channel forming region and a p-type impurity region of a fourth concentration that forms a source region or a drain region and is disposed in contact with the channel forming region;

the n-channel TFT of the driver circuit comprises a channel forming region, an n-type impurity region of a first concentration which forms a LDD region that is disposed in contact with the channel forming region and partly overlaps a gate electrode, and an n-type impurity region of a third concentration which is disposed in the outside of the n-type impurity region of the first concentration and forms a source region or a drain region;

the pixel TFT comprises a channel forming region, an n-type impurity region of a second concentration which is disposed in contact with the channel forming region and forms a LDD region, and an n-type impurity region of the third concentration which is disposed in the outside of the n-type impurity region of the second concentration and forms a source region or a drain region and

a pixel electrode disposed in the pixel section has a light reflective surface, the pixel electrode is formed over an interlayer insulating film comprising an organic insulating material, and is connected to the pixel TFT through an opening formed in a protective insulating film comprising

an inorganic insulating material disposed over a gate electrode of the pixel TFT and in the interlayer insulating film formed in contact with the protective insulating film.

3. (Amended) A semiconductor device having a liquid crystal sandwiched between a pair of substrates, wherein:

one of the substrates comprises a pixel TFT disposed in a pixel section and a p-channel TFT and an n-channel TFT of a driver circuit, wherein:

the p-channel TFT of the driver circuit comprises a channel forming region, a p-type impurity region of a fourth concentration which forms a source region or a drain region and is disposed in contact with the channel forming region;

the n-channel TFT of the driver circuit comprises a channel forming region, an n-type impurity region of a first concentration which is disposed in contact with the channel forming region and forms a LDD region that partly overlaps a gate electrode and an n-type impurity region of a third concentration which is disposed on the outside of the n-type impurity region of the first concentration and forms a source region or a drain region;

the pixel TFT comprises a channel forming region, an n-type impurity region of a second concentration which is disposed in contact with the channel forming region and forms a LDD region and an n-type impurity of the third concentration which is disposed on the outside of the n-type impurity region of the second concentration and forms a source region or a drain region;

a pixel electrode disposed in the pixel section has a light reflective surface, the pixel electrode is formed over an interlayer insulating film comprising an organic insulating material and is connected to the pixel TFT through an opening formed in a protective insulating film comprising an inorganic insulating material disposed over a gate electrode of the pixel TFT and in the interlayer insulating film formed in contact with the protective insulating film; and

said one of the substrate is stuck to the other substrate on which a transparent conductive film is formed, through at least a columnar spacer formed on superposition of the opening.

25 (Amended). A semiconductor device according to claim 1 wherein the semiconductor device is in an apparatus selected from a group consisting of a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disc player, an electronic game machine and a projector.

27 (Amended). A semiconductor device according to claim 3 wherein the semiconductor device is in an apparatus selected from a group consisting of a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disc player, an electronic game machine and a projector.

Please add new claim 53 as follows.

53. (New) A semiconductor device comprising:

a pixel TFT having disposed in a pixel section over a substrate;

a driver circuit comprising a p-channel TFT and an n-channel TFT over the substrate,

a first interlayer insulating film comprising an inorganic insulating material formed over the pixel section;

a second interlayer insulating film comprising an organic insulating material over the first interlayer insulating film;

a pixel electrode having light reflective surface over the second interlayer insulating film, and in connected to the pixel TFT through an opening formed in the first and second interlayer insulating film;

a source wiring over the second interlayer insulating film;

an alignment film formed over the pixel electrode and the source wiring; and

a liquid crystal interposed between the alignment film and an opposed substrate,

wherein:

the p-channel TFT of the driver circuit comprises a channel forming region and a p-type impurity region of a fourth concentration that forms a source region or a drain region and is disposed in contact with the channel forming region;

the n-channel TFT of the driver circuit comprises a channel forming region, an n-type impurity region of a first concentration which forms a LDD region that is disposed in contact with the channel forming region and partly overlaps a gate electrode, and an n-type impurity region of a third concentration which is disposed in the outside of the n-type impurity region of the first concentration and forms a source region or a drain region;

the pixel TFT comprises a channel forming region, an n-type impurity region of a second concentration which is disposed in contact with the channel forming region and forms a LDD region, and an n-type impurity region of the third concentration which is disposed in the outside of the n-type impurity region of the second concentration and forms a source region or a drain region;

the pixel electrode and the source wiring are formed, simultaneously.

Drawings as filed

FIG. 1A

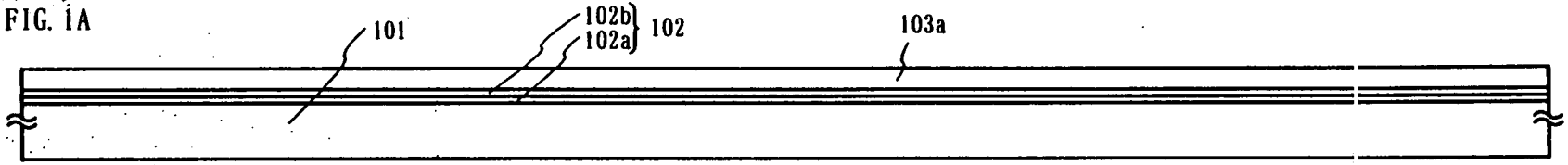
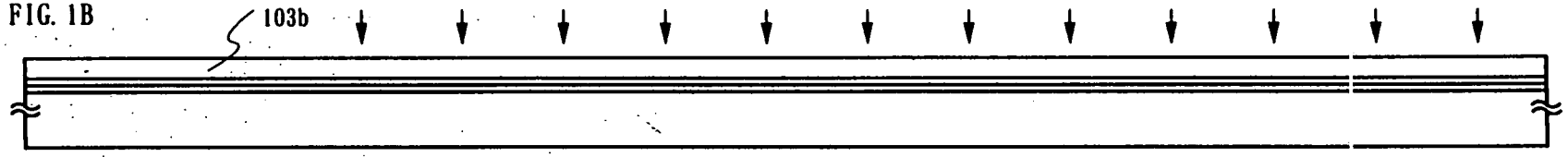


FIG. 1B



add new Fig. 1C

FIG. 1C 1D

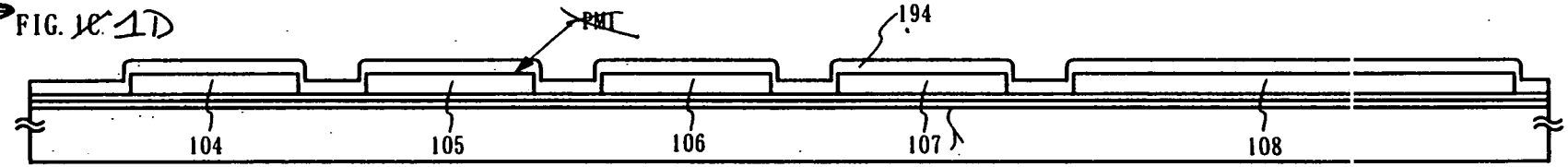


FIG. 1D 1E

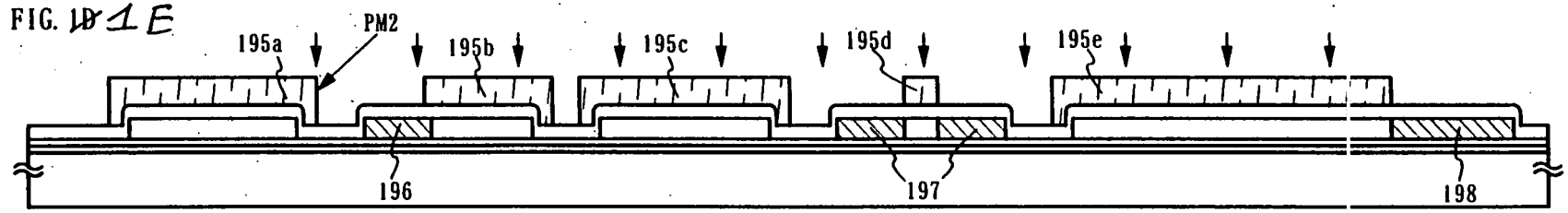


FIG. 1E 1F

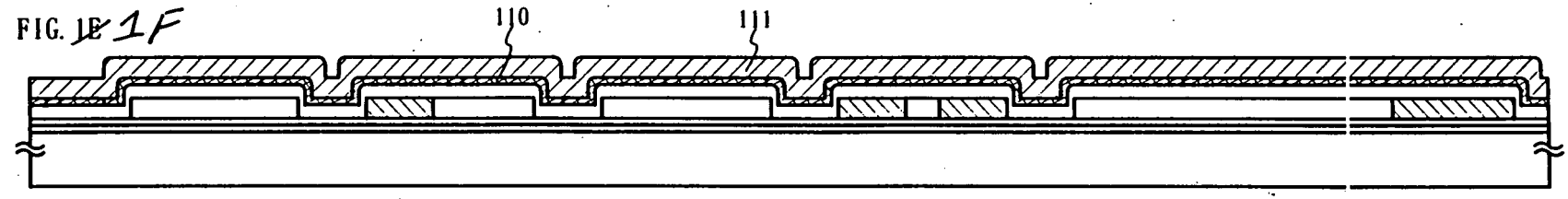


FIG. 3A

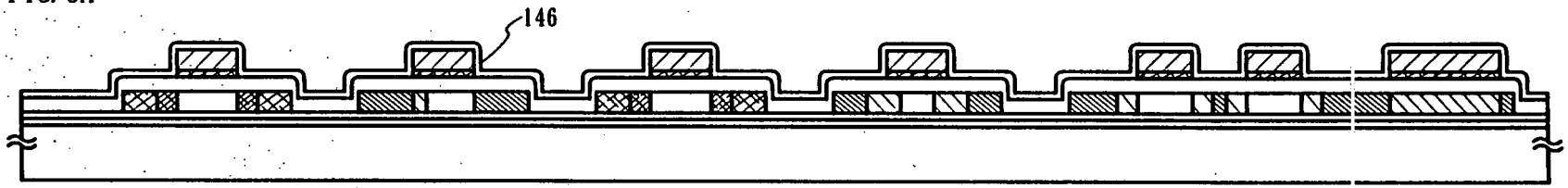
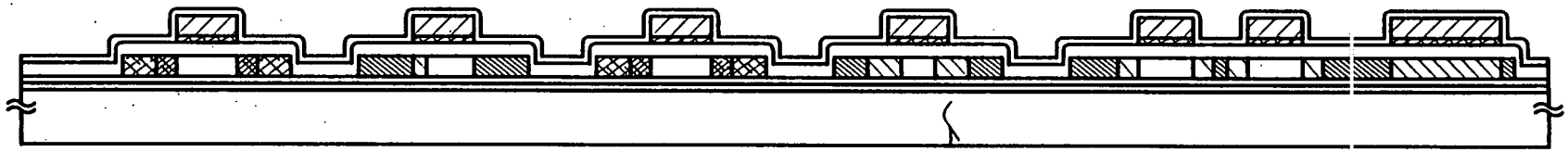
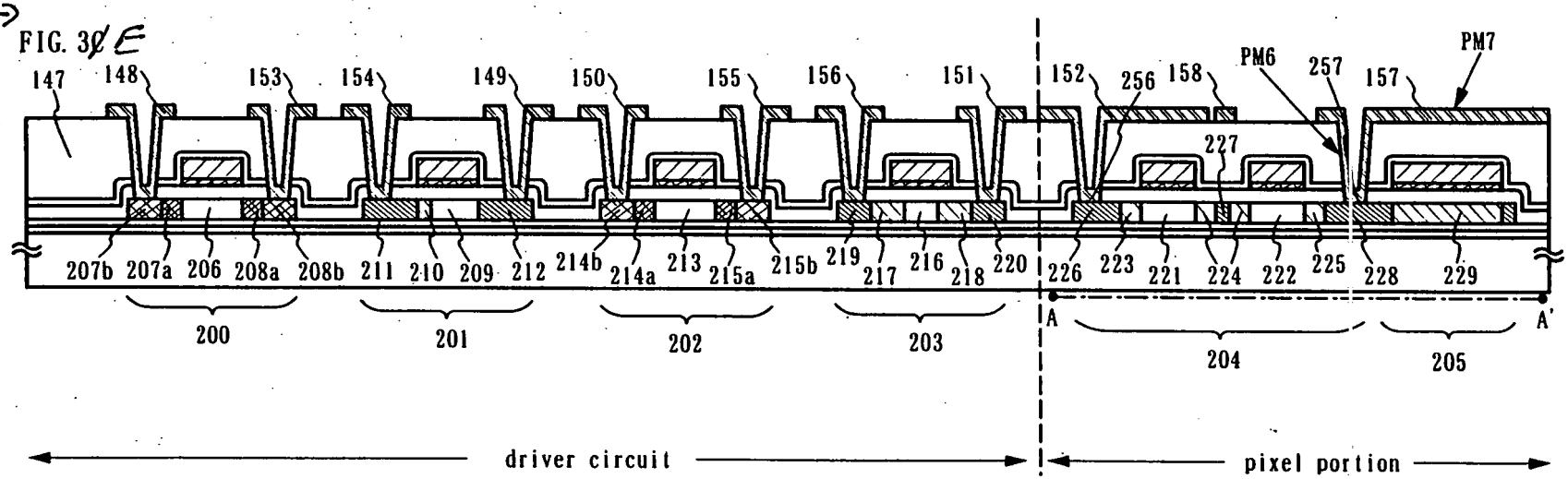


FIG. 3B



add new FIG. 3C and FIG. 3D

FIG. 3C/E



region of the p-channel TFT and the fourth concentration p-type impurity region which forms a source region or a drain region.

In the above method of manufacturing a semiconductor device, it is characterized by further comprising the steps of: forming a gate electrode of the pixel TFT and the p-channel TFT and the n-channel TFT in the periphery of the pixel portion from a heat-resistant conductive material; and forming a gate wiring from a low-resistant conductive material, extending from the driver circuit to be connected to the gate electrode. Preferably the heat-resistant conductive material is formed from an element selected from the group consisting of tantalum (Ta), titanium (Ti), molybdenum (Mo), and tungsten (W); or a compound containing the above elements; or a compound of a combination of the above elements; or a nitride compound containing the above elements; or a silicide containing the above elements.

Still further, in the above method of manufacturing a semiconductor device, it is characterized in that the columnar spacer is also formed on the p-channel TFT and the n-channel TFT of the driver circuit, and that the column-shape spacer is formed at least covering the source wiring or the drain wiring of the p-channel TFT and the n-channel TFT of the driver circuit

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A to 1E are cross-sectional views showing manufacturing steps of a pixel TFT and TFTs of a driving circuit;

Fig. 2A to 2D are cross-sectional views showing manufacturing steps of a pixel TFT and TFTs of a driving circuit;

Fig. 3A to 3E are cross-sectional views showing manufacturing steps of a pixel TFT and TFTs of a driving circuit;

Fig. 16 is a top view showing the pixel of the pixel section;

Fig. 17 is a block diagram useful for explaining the circuit construction of the liquid crystal display device;

Fig. 18 is an explanatory view of the connection structure between a flexible printed circuit board and external input/output terminals;

Fig. 19 is a cross-sectional view showing a manufacturing step of an active matrix type liquid crystal display device;

Fig. 20 is an explanatory view of the connection structure between the flexible printed board and the external input/output terminals;

Fig. 21A and 21B is a schematic view showing an example of semiconductor devices;

Fig. 22A to 22F are diagrams showing an example of the semiconductor devices; and

Fig. 23A to 23D are diagrams showing an example of the projection type liquid crystal display devices.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, preferred embodiments of the present invention will be explained in detail.

[Embodiment 1]

An embodiment of the present invention will be explained with reference to Figs. 1A to 5F. In this embodiment, a method of forming simultaneously pixel TFTs and storage capacitors of a pixel section and TFTs of a driving circuit disposed in the periphery of the display region will be explained step-wise in detail.

In Fig. 1A, as well as barium borosilicate glass or aluminoborosilicate glass as

semiconductor layer 103b can be formed by the crystallization method using a catalytic element in accordance with the technology disclosed in Japanese Patent Application Laid-Open No. 7-130652. In the crystallization step, hydrogen contained in the amorphous semiconductor layer is first discharged preferably. It is good to perform the crystallization step after heat-treatment is conducted at 400 to 500°C for about 1 hour to lower the hydrogen content to 5 atom% or below, because roughness of the film surface can be prevented advantageously.

When the crystallization step is conducted by the laser annealing method, a pulse oscillation type or continuous light emission type excimer laser, or an argon laser is used as the light source. When the pulse oscillation type excimer laser is used, the laser beam is processed to a linear shape and laser annealing is then conducted. The laser annealing condition can be selected appropriately by the operator. For example, the laser pulse oscillation is 30 Hz and the laser energy density is 100 to 500 mJ/cm^2 (typically, 300 to 400 mJ/cm^2). The linear beams are irradiated to the entire surface of the substrate, and the overlap ratio of the linear beams at this time is 80 to 98%. In this way, the crystalline semiconductor layer 103b can be obtained as shown in Fig. 1B.

A resist pattern is formed on the crystalline semiconductor layer 103b by photolithography that uses a photo-mask 1 (PM1). The crystalline semiconductor shown in Fig. 1C layer is divided into an island shape by dry etching, forming thereby island semiconductor layers 104 to 108. A mixed gas of CF_4 and O_2 is used for dry etching. A mask layer 194 is then formed from a silicon oxide film having 50 to 100 nm thickness by plasma-enhanced CVD or sputtering.

An impurity for imparting the p-type may be applied in a concentration of about 1 x 10^{16} to 5 x 10^{17} atoms/cm^3 to the entire surface of the island semiconductor layers of this state to control the threshold voltage (Vth) of the TFTs. The elements of

with the oscillating frequency set between 5 and 50 Hz, the energy density set between 100 and 500 mJ/cm^2 to scan at an overlapping ratio of between 80% and 98% to thereby treat the entire surface of the substrate on which the island-like semiconductor layer is formed. Note that there are no limitations placed on the irradiation conditions of the laser light, appropriate irradiation conditions may be determined by an operator. The mask layer 194 is removed by etching with a solution such as fluorine.

A gate insulating film 109 is formed from an insulating film containing silicon at a film thickness of between 40 and 150 nm by plasma CVD or sputtering. For example, it is appropriate to form the gate insulating film at a thickness of 120 nm from a silicon oxide nitride film. In addition, a silicon oxide nitride film made from SiH_4 and N_2O, both doped with O_2, is a favorable material for the application here because the fixed electric charge density has been reduced. The gate insulating film, of course, is not limited to such silicon oxide nitride film. A single layer or a laminated layer of other insulating films containing silicon may be used. (See Fig. 1E)

As shown in Fig. 1F, a heat-resistant conductive layer, for forming a gate electrode on the gate insulating film 109, is formed. The heat-resistant conductive layer may be formed as a single layer, or if necessary, it may have a laminated structure formed of a plurality of layers, such as 2 or 3 layers. Using such heat-resistant conductive materials, a lamination structure of, for example, a conductive layer (A) 110 formed from a conductive nitride metallic film and a conductive layer (B) 111 formed from a metallic film, is appropriate. The conductive layer (B) 111 may be formed from an element selected from the group consisting of tantalum (Ta), titanium (Ti), molybdenum (Mo), and tungsten (W); or an alloy having the above elements as its principal constituent; or an alloy film formed from a combination of the above elements (typically, an Mo-W alloy film and an Mo-Ta alloy film). The conductive layer (A) 110

silicon oxide nitride film or the silicon nitride film formed as the protective insulating film 146 as in this embodiment. shown in Fig. 3C

Thereafter, a resist mask having a prescribed pattern is formed by using a photo-mask 6 (PM6), and contact holes reaching the source or drain regions of the respective island semiconductor films are formed. The contact holes are formed by dry etching. In this case, a mixed gas of CF_4, O_2 and He is used as the etching gas to first etch the interlayer insulating film formed of the organic resin material. The protective insulation film 146 is then etched with etching gases of CF_4 and O_2. By switching the etching gas further to CHF_3 to improve the selection ratio with the island semiconductor layers, the gate insulating film is etched and the contact holes can be formed satisfactorily.

A conductive metal film is formed by sputtering or vacuum deposition. A resist mask pattern is then formed by using a photo-mask 7(PM7). shown in Fig. 3D Source wirings 148 to 152 and drain wirings 153 to 158 are formed by etching. Here, the drain wiring 157 functions as the pixel electrode. Though not shown in the drawing, in this embodiment, Ti film is formed into 50 to 150 nm thickness, a contact is formed with the semiconductor film that forms source or drain region in the island semiconductor layer, and aluminum (Al) is formed to a thickness of 300 to 400 nm in superposition with the Ti film to give this wiring.

When the hydrogenation treatment is conducted under this state, favorable results can be obtained for the improvement of TFT performance. For example, the heat-treatment is conducted preferably at 300 to 450°C for 1 to 12 hours in an atmosphere containing 3 to 100% of hydrogen. A similar effect can be obtained by using the plasma hydrogenation method. Such a heat-treatment can diffuse hydrogen existing in the protective insulating film 146 and the base film 102 into the island

semiconductor films 104 to 108 and can hydrogenate these films. In any case, the defect density in the island semiconductor films 104 to 108 is lowered preferably to $10^{16}/cm^3$ or below, and for this purpose, hydrogen may be added in an amount of about 0.01 to about 0.1 atomic% (Fig. 3E).

Thus a substrate having the TFTs of the driving circuit and the pixel TFTs of the pixel section over the same substrate can be completed with 7 photo-masks. The first p-channel TFT 200, the first n-channel TFT 201, the second p-channel TFT 202 and the second n-channel TFT 203 are formed in the driving circuit. The pixel TFT 204 and the storage capacitance 205 are formed in the pixel section. In this specification, such a substrate will be referred to as an "active matrix substrate" for convenience sake.

The first p-channel TFT 200 in the driving circuit has a single drain structure, which has in the island semiconductor film 104: the channel formation region 206; and the source regions 207a and 207b and the drain regions 208a and 208b each comprising the p-type impurity region having the fourth concentration. The first n-channel TFT 201 has in the island semiconductor film 105: the channel forming region 209; the LDD region 210 that partly overlaps with the gate electrode 119 and comprises the impurity region having the first concentration; and the source region 212 and the drain region 211 comprising the impurity region having the third concentration. The LDD region that overlaps the gate electrode 119 is referred to as Lov here, and the length of this region in the direction of the channel length is 0.5 to 3.0 μm, preferably 1.0 to 2.0 μm. As the length of the LDD region in the n-channel TFT is determined in this way, a high electric field generated in the proximity of the drain region can be mitigated, and the occurrence of hot carriers and degradation of the TFT can be prevented. The second p-channel TFT 202 in the driving circuit has similarly the single drain structure including the

channel forming region 213, the source regions 214a and 214b and the drain regions 215a and 215b comprising the p-type impurity region having the fourth concentration, in the island semiconductor film 106. A channel forming region 216; LDD regions 217 and 218 that partly overlap the gate electrode 121 and comprises the impurity region of the first concentration; and a source region 220 and a drain region 219 comprising the impurity region of the third concentration; are formed in the second n-channel TFT 203. The length of the Lov that partly overlaps the gate electrode of this TFT, too, is also set to 0.5 to 3.0 μm, preferably from 1.0 to 2.0 μm. Further, a LDD region that does not overlap the gate electrode is referred to as an Loff region, and its length in the channel length direction is 0.5 to 4.0 μm, preferably 1.0 to 2.0 μm. The pixel TFT 204 has in the island semiconductor film 108: channel forming regions 221 to 222; and LDD regions 223 to 225 comprising an impurity region of the second concentration; and source or drain regions 226 to 228 comprising an impurity region of the third concentration. The length of the LDD region (Loff) in the direction of the channel length is 0.5 to 4.0 μm, preferably 1.5 to 2.5 μm. Furthermore, a storage capacitance 205 comprises a capacitance wiring 123, an insulating film made of the same material as the gate insulating film and a semiconductor layer 229 that is connected to the drain region 228 of the pixel TFT 204. In Fig. 3E the pixel TFT 204 is shown as having a double gate structure. However, it may have a single gate structure or a multi-gate structure having a plurality of gate electrodes.

Fig. 16 is a top view showing substantially one pixel of the pixel section. The cross section A – A' in the drawing corresponds to the sectional view of the pixel section shown in Fig. 3E. The gate electrode 122 of the pixel TFT 204, that functions also the gate wiring, intersects the island semiconductor layer 108 below it through a gate insulating film, which is not shown in the drawing. The source region, the drain